FIG. 1

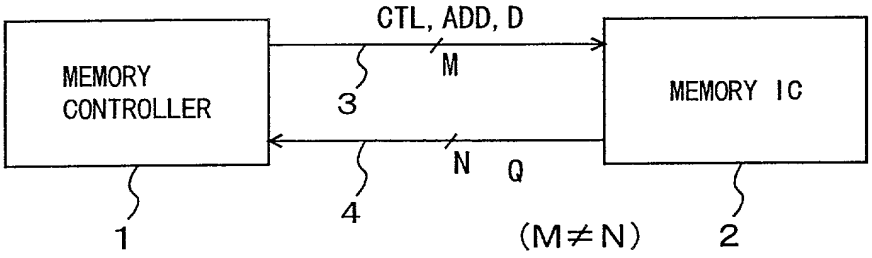
CTL, ADD, D
M
MEMORY CONTROLLER
3
MEMORY IC
N
Q
4
1
(M≠N)
2

FIG. 2

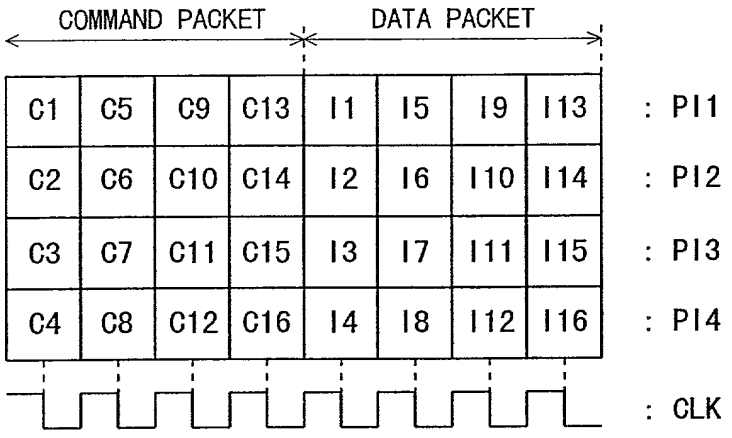
COMMAND PACKET
DATA PACKET
C1 C5 C9 C13 I1 I5 I9 I13 : PI1
C2 C6 C10 C14 I2 I6 I10 I14 : PI2
C3 C7 C11 C15 I3 I7 I11 I15 : PI3
C4 C8 C12 C16 I4 I8 I12 I16 : PI4
: CLK

FIG. 3

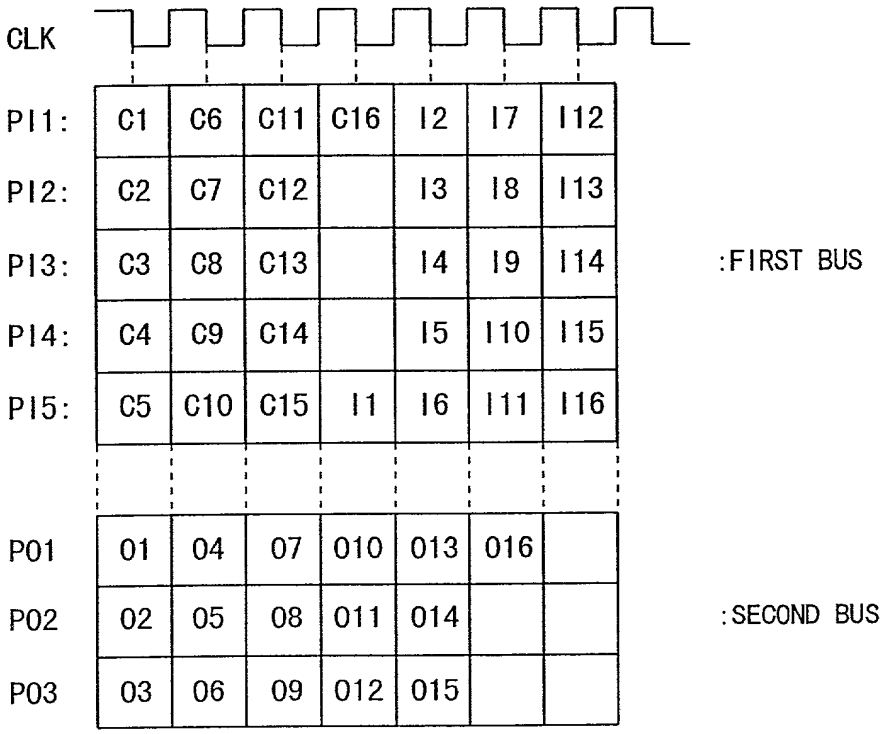
CLK
PI1: C1 C6 C11 C16 I2 I7 I12
PI2: C2 C7 C12 I3 I8 I13
PI3: C3 C8 C13 I4 I9 I14
PI4: C4 C9 C14 I5 I10 I15
PI5: C5 C10 C15 I1 I6 I11 I16
:FIRST BUS
P01 01 04 07 010 013 016
P02 02 05 08 011 014
P03 03 06 09 012 015
:SECOND BUS

FIG. 4

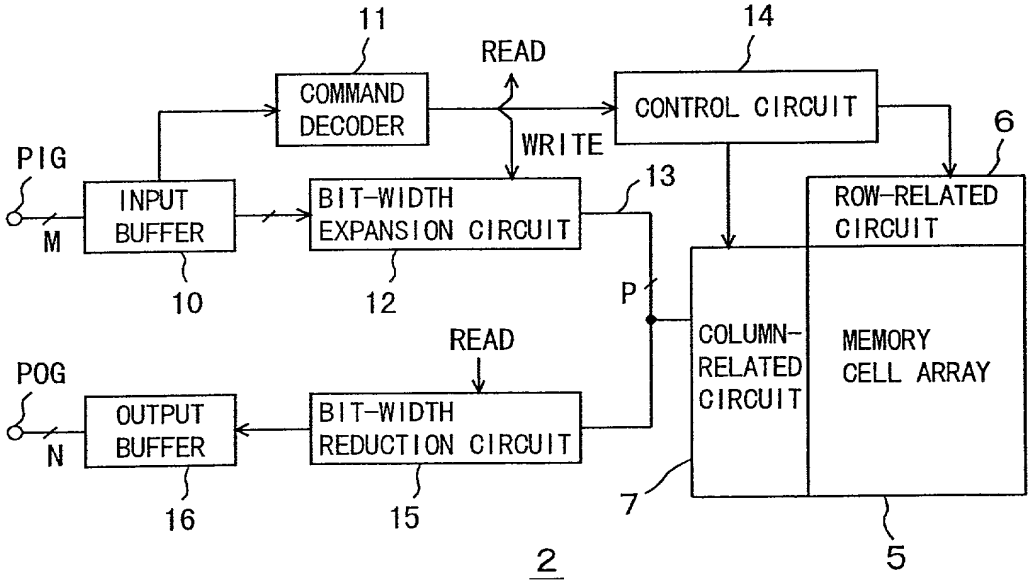
11
COMMAND DECODER
READ
WRITE
14
CONTROL CIRCUIT
6
PIG
M
INPUT BUFFER
10
BIT-WIDTH EXPANSION CIRCUIT
12
13
ROW-RELATED CIRCUIT
P
READ
POG
N
OUTPUT BUFFER
16
BIT-WIDTH REDUCTION CIRCUIT
15
COLUMN-RELATED CIRCUIT
7
MEMORY CELL ARRAY
5
2

FIG. 5

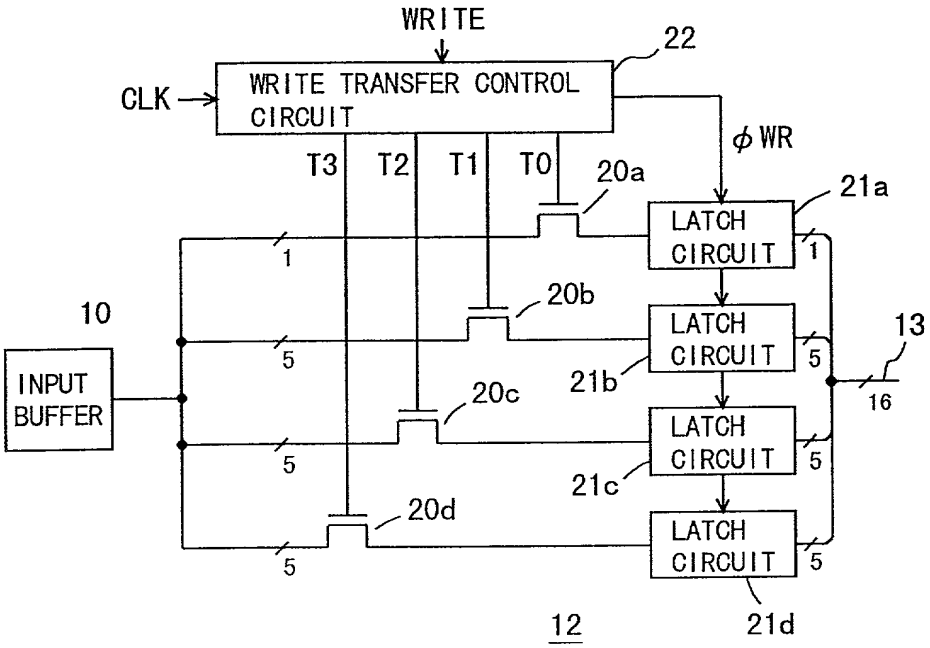
WRITE
22
CLK
WRITE TRANSFER CONTROL CIRCUIT
φWR
T3
T2
T1
T0
20a
21a
LATCH CIRCUIT
1
20b
10
5
LATCH CIRCUIT
13
INPUT BUFFER
21b
20c
16
LATCH CIRCUIT
21c
20d
LATCH CIRCUIT
21d
12

FIG. 6

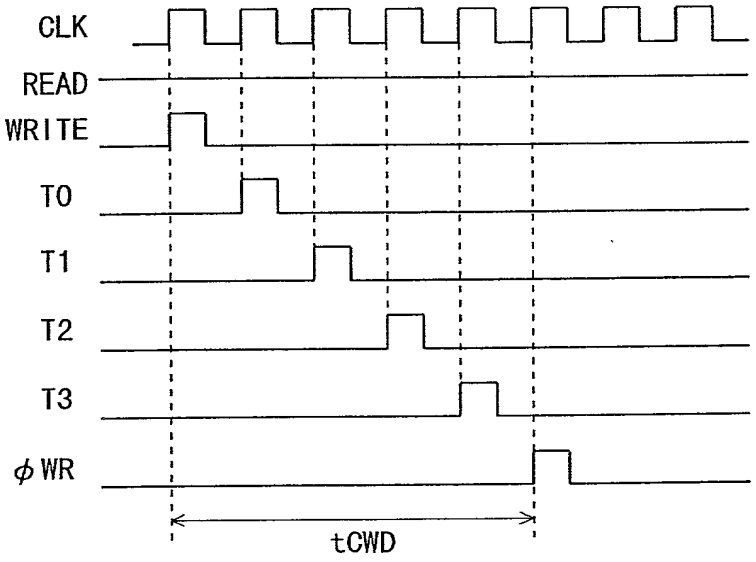
CLK
READ
WRITE
T0
T1
T2
T3
φWR
tCWD

FIG. 7A

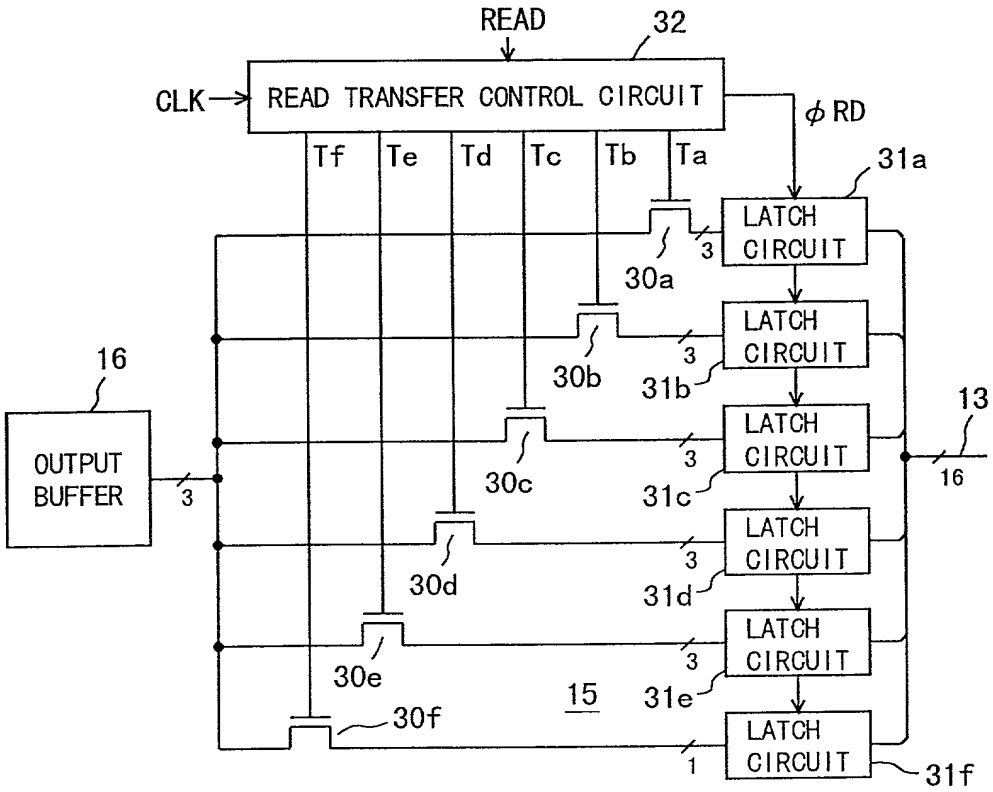
READ
32
CLK
READ TRANSFER CONTROL CIRCUIT
φRD
Tf
Te
Td
Tc
Tb
Ta
31a
LATCH CIRCUIT
3
30a
30b
31b
16
OUTPUT BUFFER
30c
31c
13
16
30d
31d
30e
31e
15
30f
1
31f

FIG. 7B

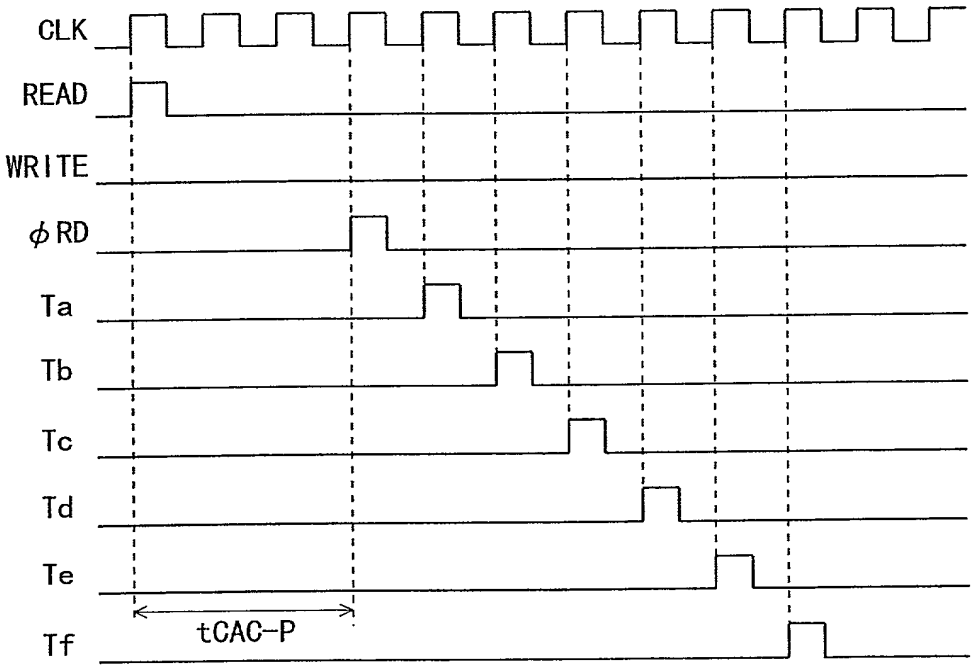
CLK
READ
WRITE
φRD
Ta
Tb
Tc
Td
Te
Tf
tCAC-P

FIG. 8

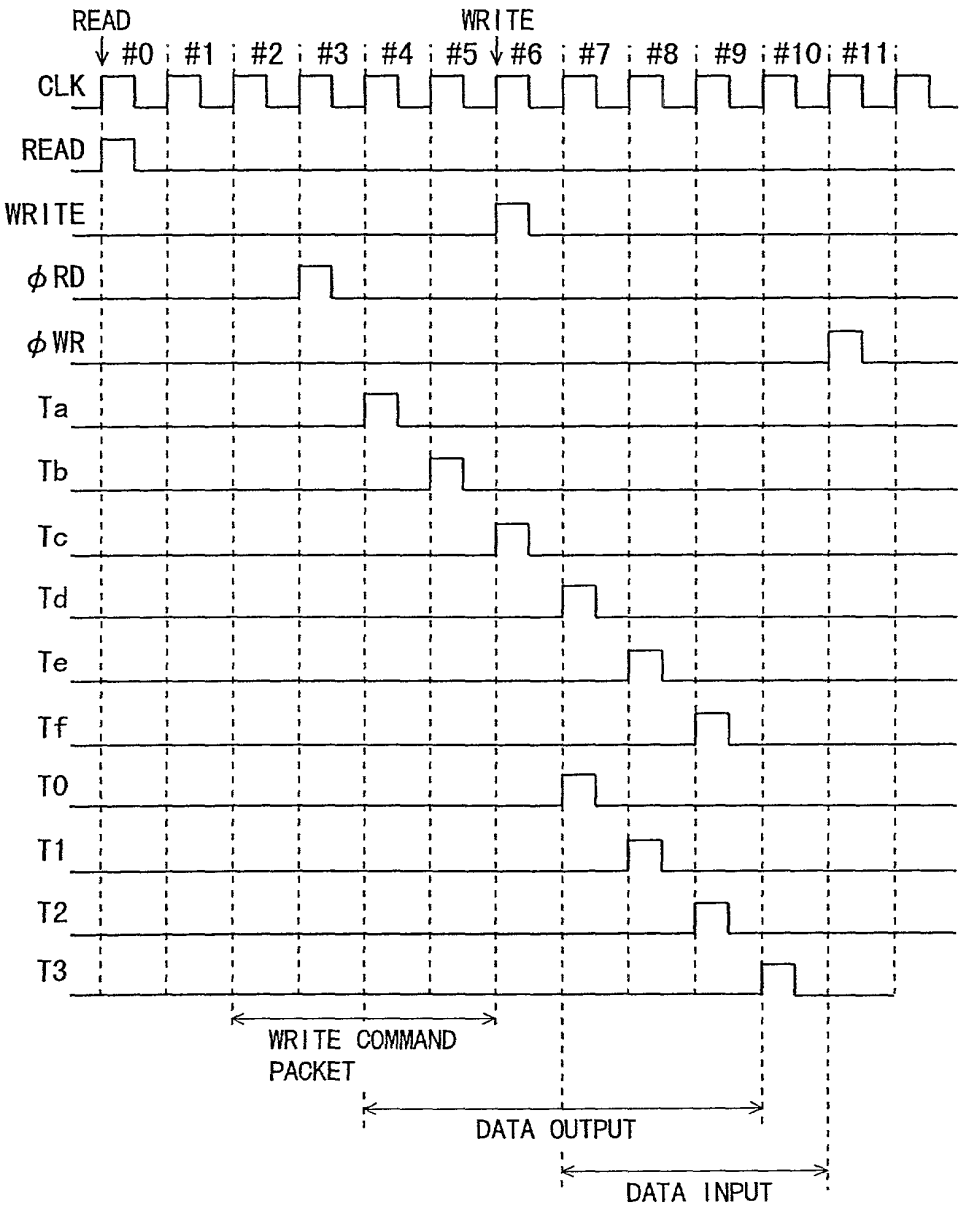
READ
WRITE
#0
#1
#2
#3
#4
#5
#6
#7
#8
#9
#10
#11
CLK
READ
WRITE
φRD
φWR
Ta
Tb
Tc
Td
Te
Tf
T0
T1
T2
T3
WRITE COMMAND PACKET
DATA OUTPUT
DATA INPUT

FIG. 9

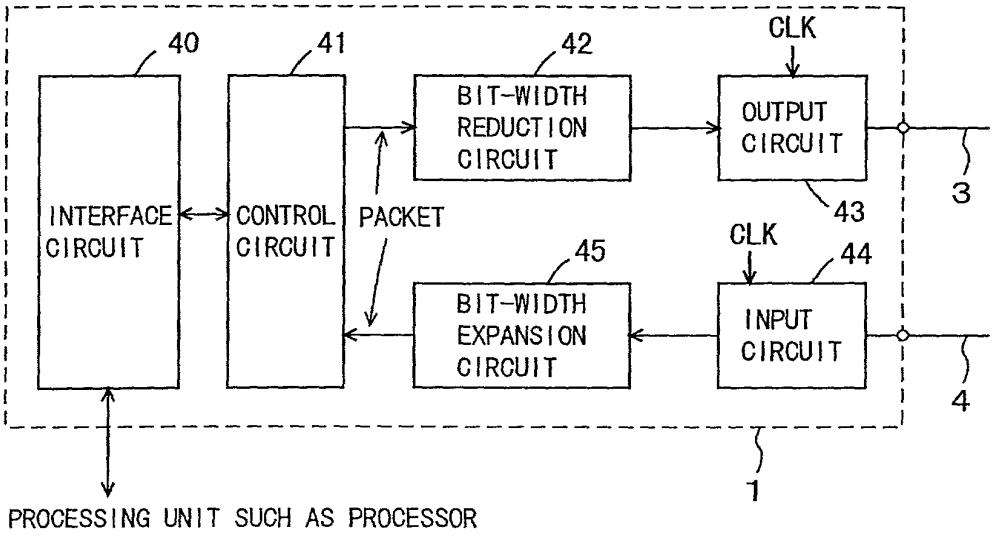
40
41
42
CLK
BIT-WIDTH REDUCTION CIRCUIT
OUTPUT CIRCUIT
INTERFACE CIRCUIT
CONTROL CIRCUIT
PACKET
43
3
CLK
45
44
BIT-WIDTH EXPANSION CIRCUIT
INPUT CIRCUIT
4
1
PROCESSING UNIT SUCH AS PROCESSOR

FIG. 10

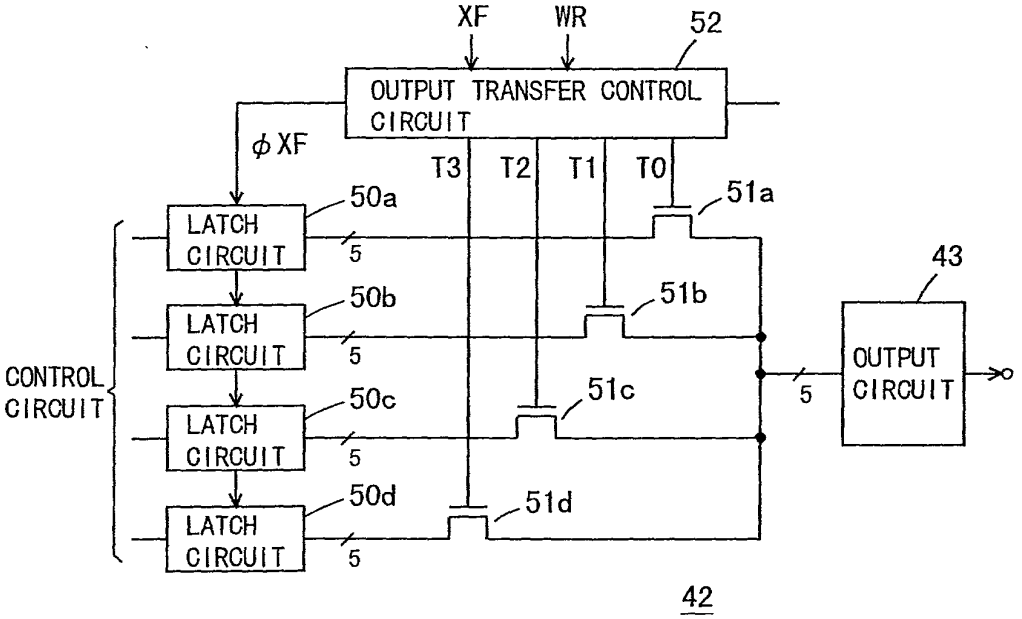
XF
WR
52
OUTPUT TRANSFER CONTROL CIRCUIT
φXF
T3
T2
T1
T0
50a
51a
LATCH CIRCUIT
5
50b
51b
43
CONTROL CIRCUIT
50c
51c
OUTPUT CIRCUIT
50d
51d
42

FIG. 11

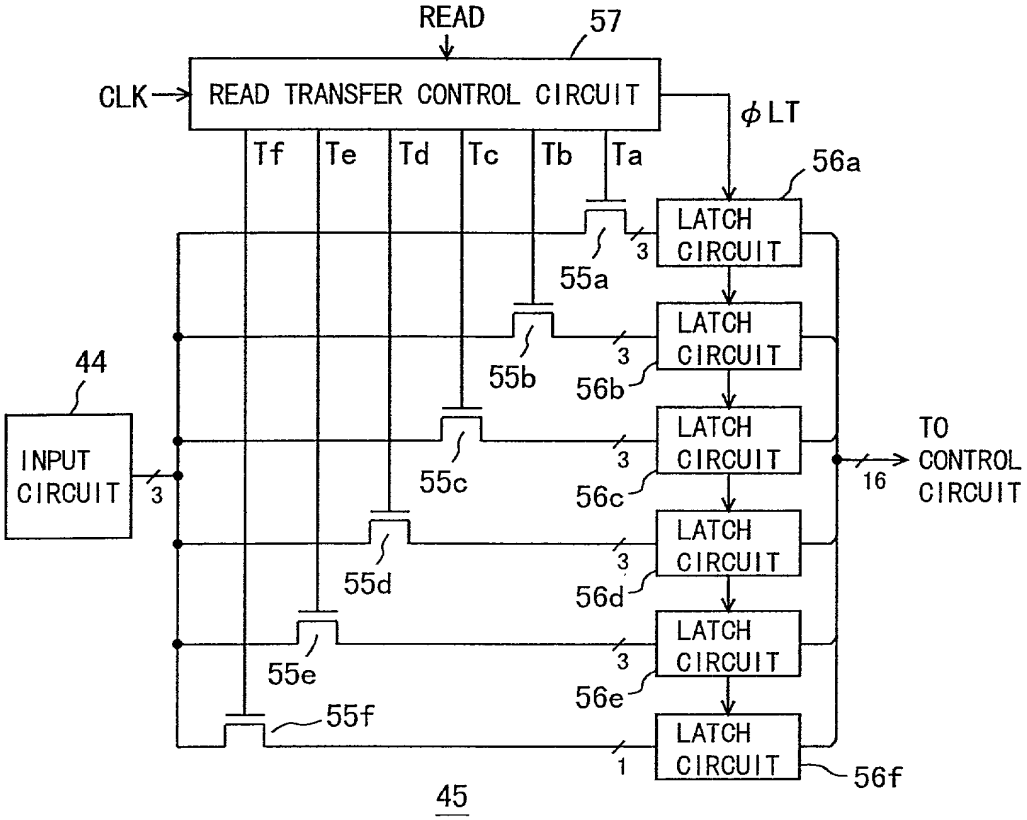
READ
57
CLK
READ TRANSFER CONTROL CIRCUIT
φLT
Tf
Te
Td
Tc
Tb
Ta
56a
LATCH CIRCUIT
3
55a
55b
56b
44
INPUT CIRCUIT
55c
56c
TO CONTROL CIRCUIT
16
55d
56d
55e
56e
55f
1
56f
45

FIG. 12

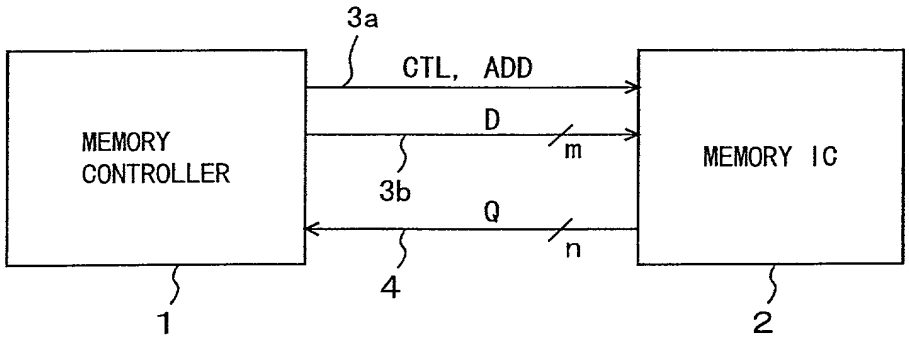
3a
CTL, ADD
D
m
MEMORY CONTROLLER
MEMORY IC
3b
Q
n
4
1
2

FIG. 13

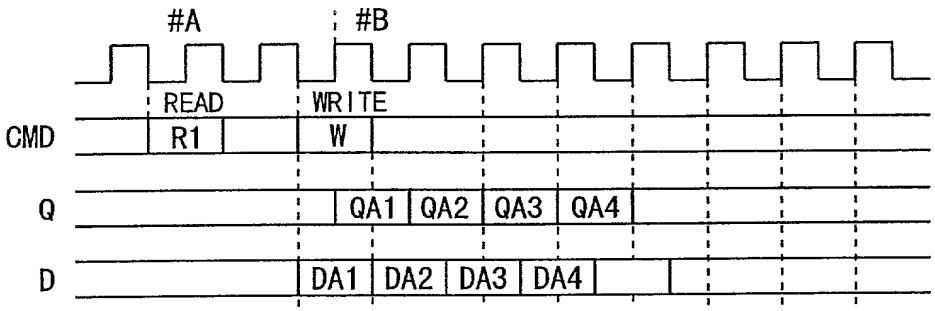
#A
#B
READ
WRITE
CMD
R1
W
Q
QA1
QA2
QA3
QA4
D
DA1
DA2
DA3
DA4

FIG. 14

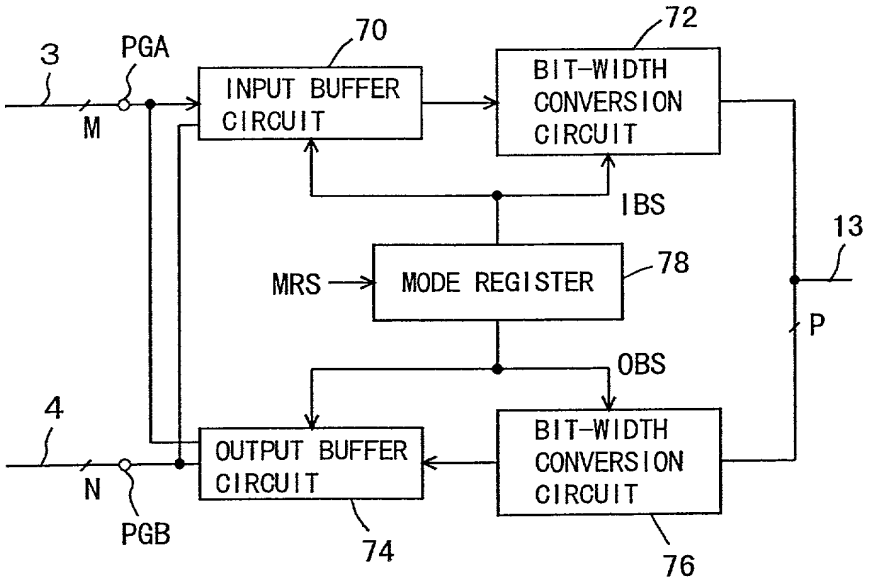
3
PGA
M
70
INPUT BUFFER CIRCUIT
72
BIT-WIDTH CONVERSION CIRCUIT
IBS
13
MRS
MODE REGISTER
78
P
OBS
4
N
PGB
OUTPUT BUFFER CIRCUIT
74
BIT-WIDTH CONVERSION CIRCUIT
76
2

FIG. 15

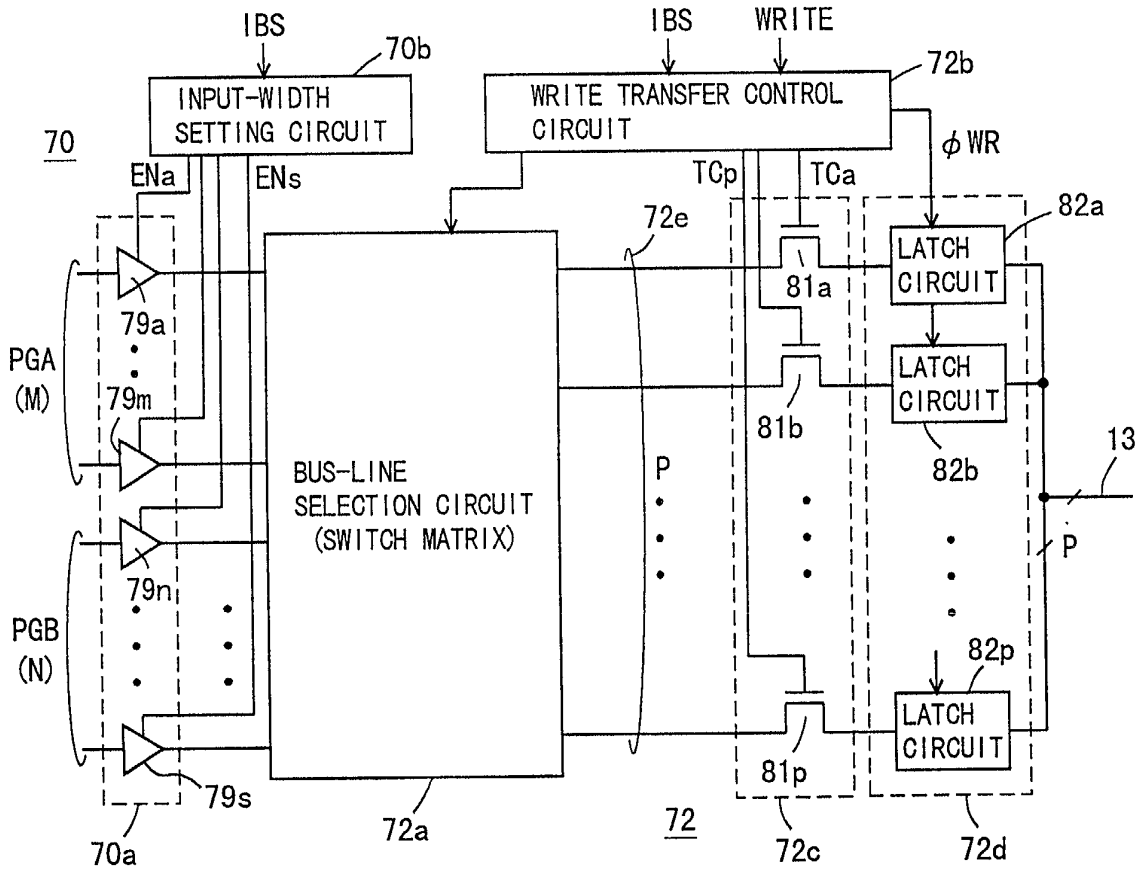

FIG. 16

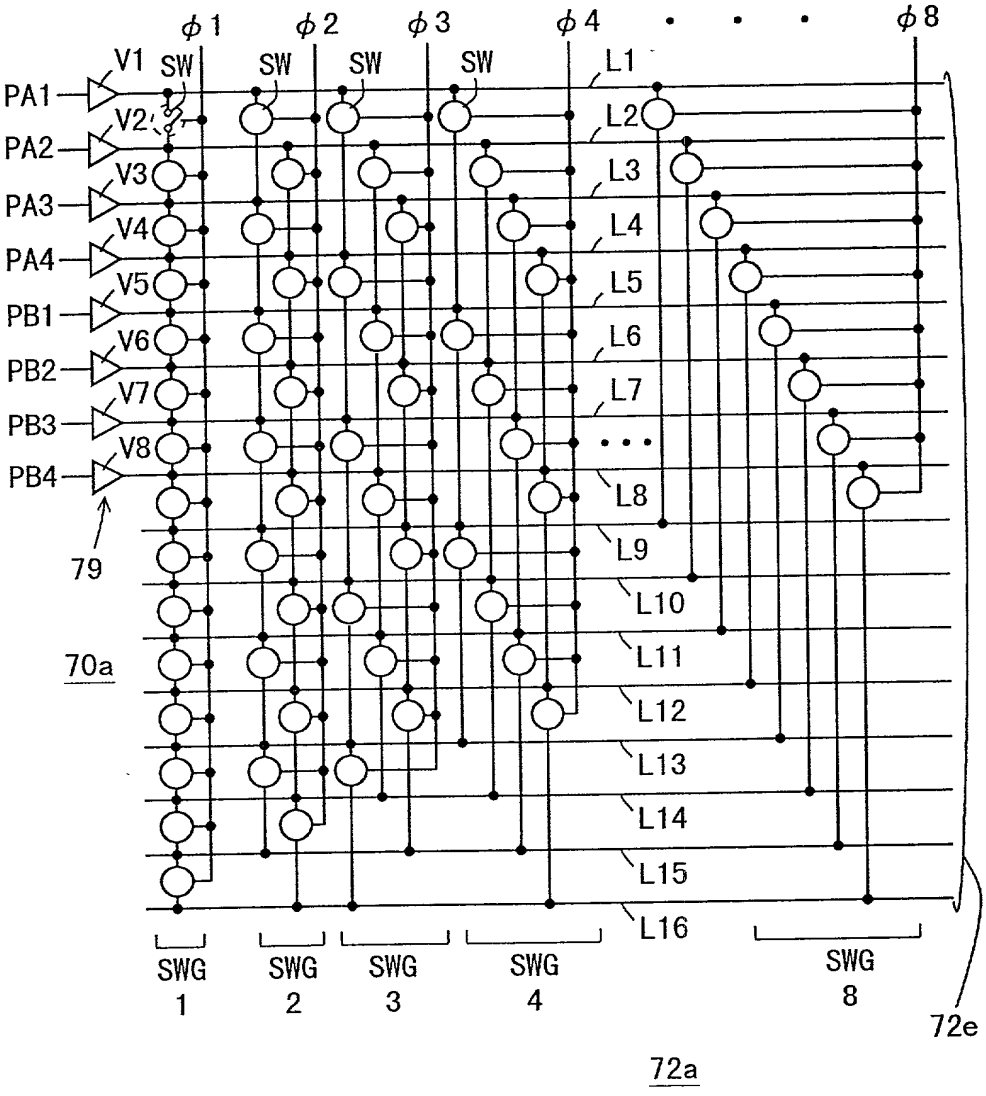
φ1
φ2
φ3
φ4
φ8
V1
SW
PA1
V2
PA2
V3
PA3
V4
PA4
V5
PB1
V6
PB2
V7
PB3
V8
PB4
79
70a
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
SWG 1
SWG 2
SWG 3
SWG 4
SWG 8
72e
72a

FIG. 17

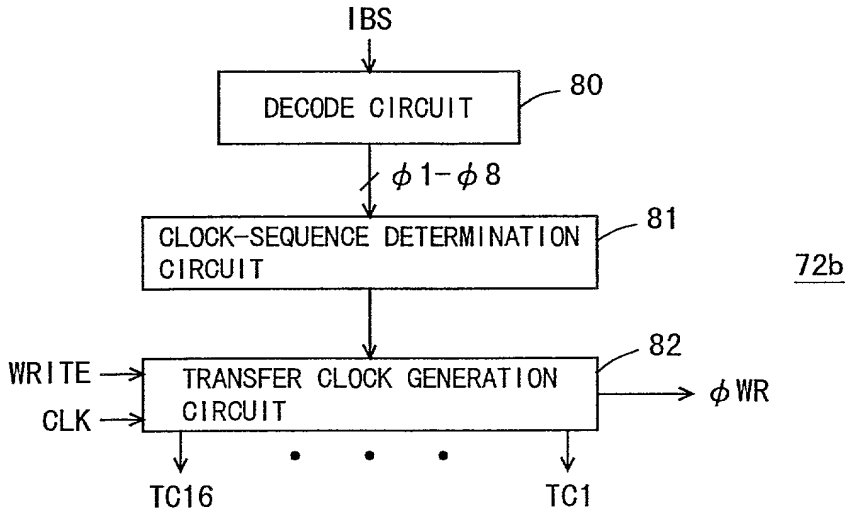

FIG. 23 PRIOR ART

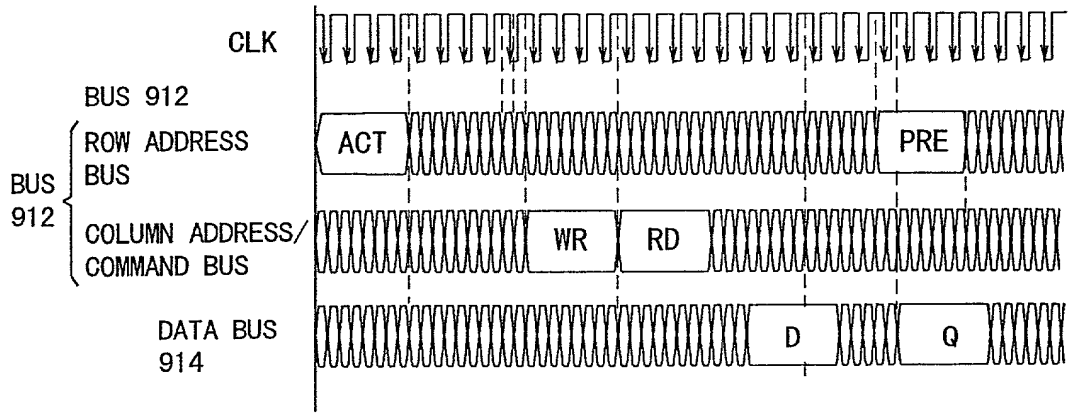

FIG. 18

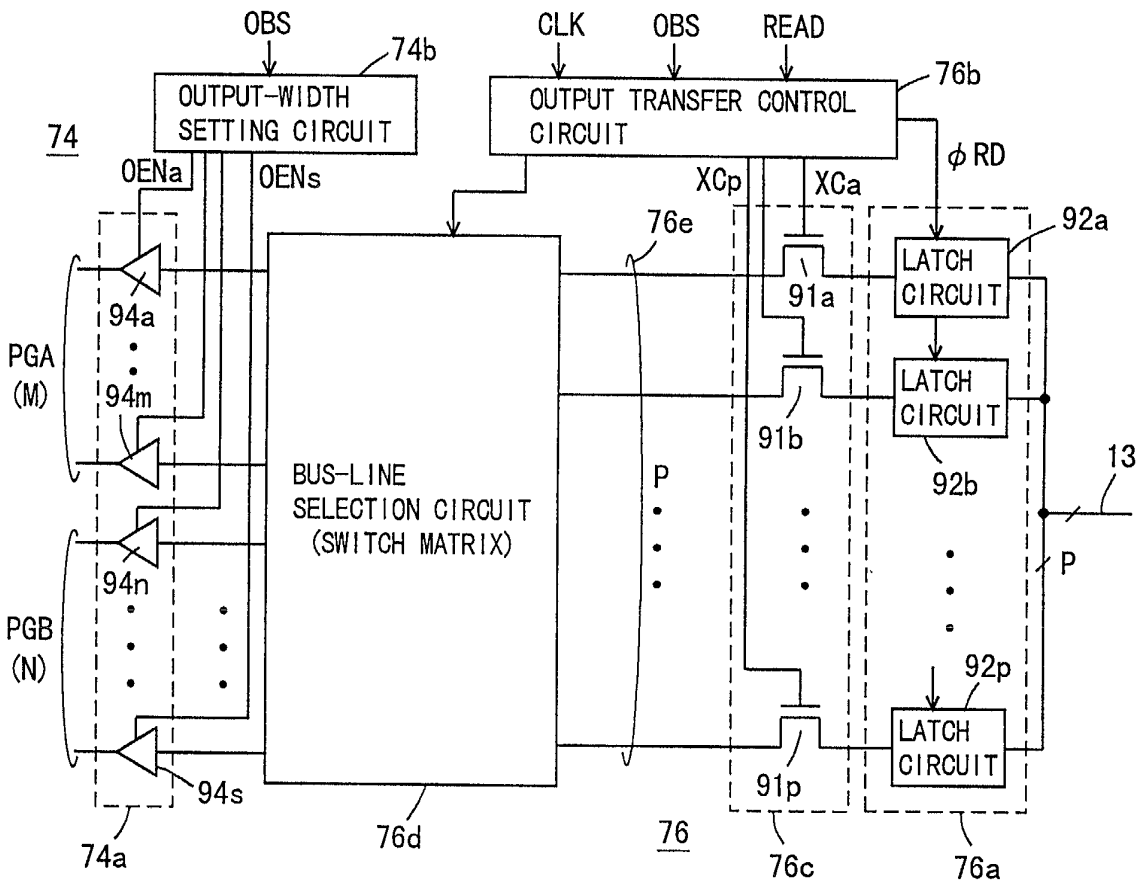

FIG. 19

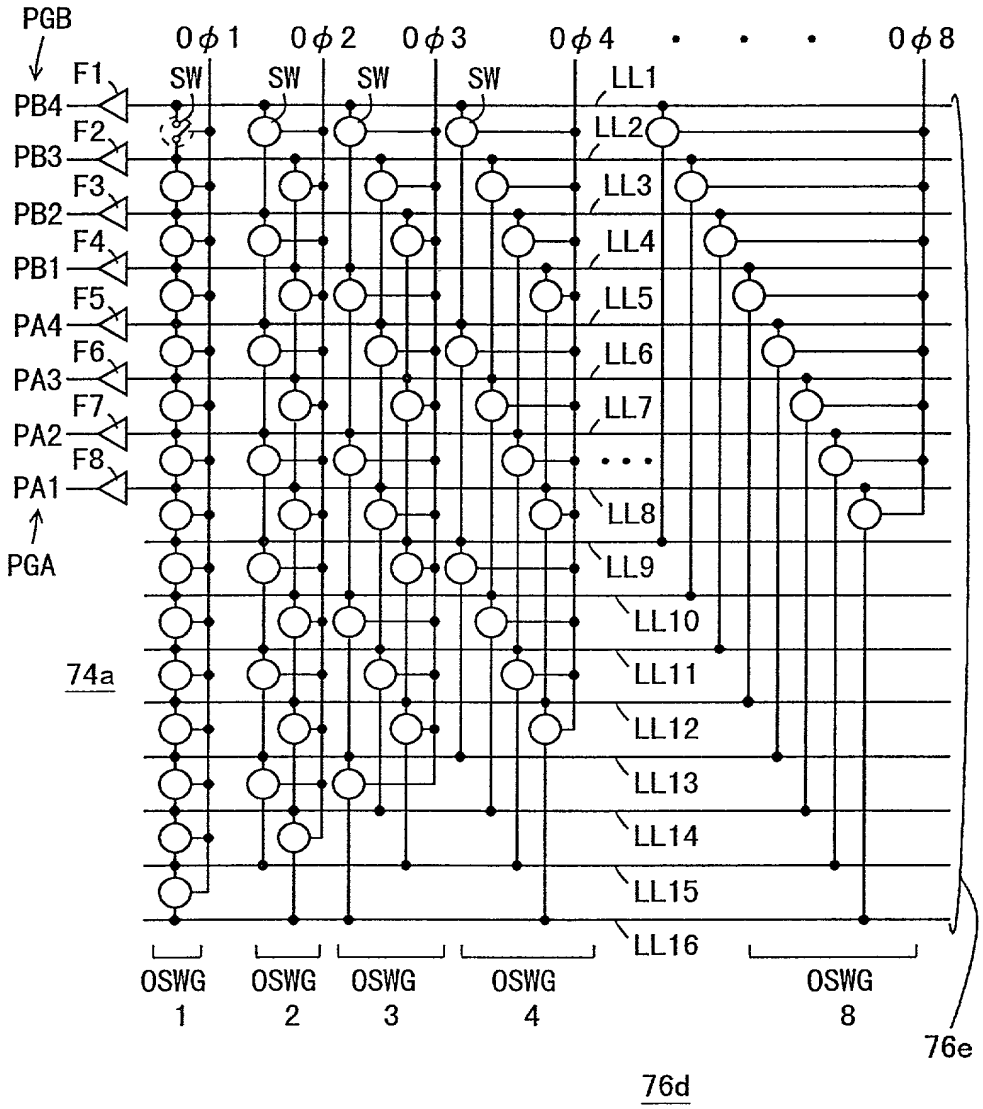
PGB
0φ1
0φ2
0φ3
0φ4
0φ8
F1
SW
LL1
PB4
F2
LL2
PB3
F3
LL3
PB2
F4
LL4
PB1
F5
LL5
PA4
F6
LL6
PA3
F7
LL7
PA2
F8
LL8
PA1
LL9
PGA
LL10
74a
LL11
LL12
LL13
LL14
LL15
LL16
OSWG 1
OSWG 2
OSWG 3
OSWG 4
OSWG 8
76e
76d

FIG. 20

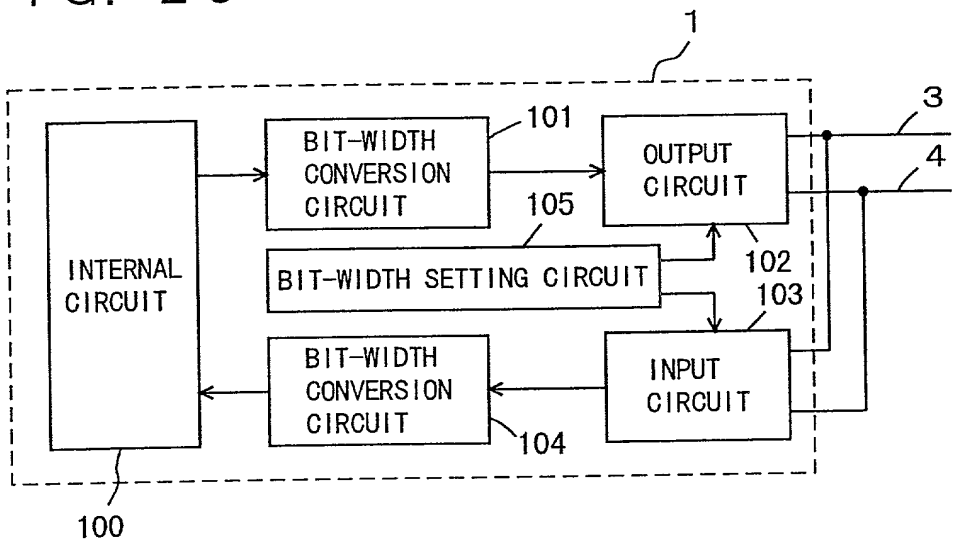

FIG. 21 PRIOR ART

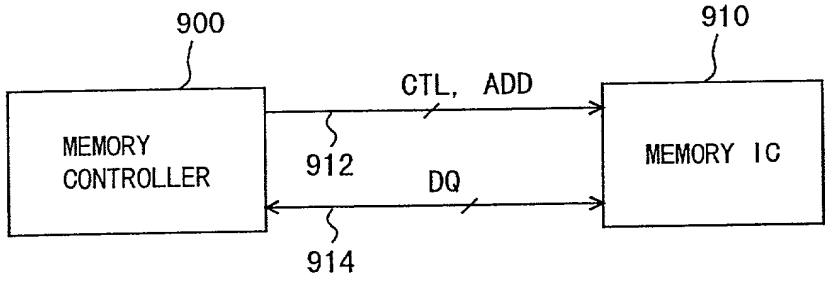

FIG. 22 PRIOR ART